

10/517, 075

Rec'd PCT/PTO 06 DEC 2004

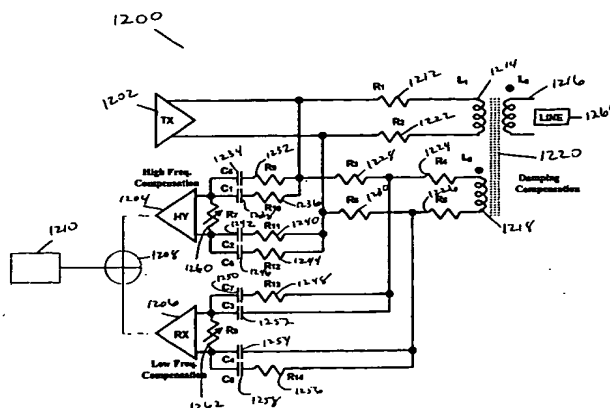
(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau(43) International Publication Date
18 December 2003 (18.12.2003)

PCT

(10) International Publication Number
WO 03/105369 A1

- (51) International Patent Classification⁷: **H04B 7/005**, 3/20, H04M 1/00, 9/08, H04L 5/16
- (21) International Application Number: PCT/US03/18127
- (22) International Filing Date: 6 June 2003 (06.06.2003)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
60/387,303 7 June 2002 (07.06.2002) US
60/387,098 7 June 2002 (07.06.2002) US
60/398,860 25 July 2002 (25.07.2002) US
60/403,874 16 August 2002 (16.08.2002) US
- (71) Applicant (for all designated States except US): **TOKYO ELECTRON LIMITED [JP/JP]**; TBS Broadcast Center, 3-6 Akasaka 5-chome, Minato-ku, Tokyo 107-8481 (JP).
- (72) Inventor; and
- (75) Inventor/Applicant (for US only): **HENCH, John, J.** [US/US]; 15297 Charmeran Avenue, San Jose, CA 95124 (US).
- (54) Title: METHOD AND SYSTEM FOR PROVIDING AN ANALOG FRONT END FOR MULTILINE TRANSMISSION IN COMMUNICATION SYSTEMS
- (57) Abstract: A method and system for providing an analog front end for multiline transmission in communications systems are described. A transceiver circuit (1100) is configured to reduce line noise by providing a coupled transmitter (1106), receiver (1106), prebalance circuit (1110), and transformer (1220) further coupled to a communication line (1264) external to the transceiver circuit. A hybrid (HY) input stage (1204) coupled to the prebalance circuit provides high frequency compensation by including a first high pass circuit coupled to the HY stage inputs, wherein the high pass circuit includes two parallel passes, each with a capacitor (C1,C5) in series with a resistor (R9,R10). A receiver input stage (RX) (RX) (1206) further coupled to the prebalance circuit provides low frequency compensation by including a second high pass circuit coupled to the RX stage inputs, wherein the high pass circuit includes two parallel passes, one with a capacitor (C3) and one with a capacitor (C7) in series with a resistor (R13). Lastly, a summing junction (1208) coupled to the HY stage (1204) and RX stage (1206) subtracts the HY stage output from the RX stage output providing a filtered incoming analog signal for post processing.
- (74) Agent: **DUTTA, Sanjeet, K.**; Blakely, Sokoloff, Taylor & Zafman LLP, 12400 Wilshire Boulevard, Seventh Floor, Los Angeles, CA 90025 (US).
- (81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).
- Published:
— with international search report
— with amended claims
- For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.



WO 03/105369 A1